The listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A method of fabricating an integrated circuit device, comprising:

forming a gate on an integrated circuit substrate, the gate having sidewalls;

forming a barrier layer spacer on the sidewalls of the gate, a portion of the barrier layer spacer protruding from the sidewalls of the gate exposing a lower surface of the barrier layer spacer that faces the integrated circuit substrate; and

forming a silicide layer on the portion of the barrier layer spacer protruding from the sidewalls of the gate.

2. (Original) The method according to Claim 1, further comprising forming source and drain regions in the integrated circuit substrate, wherein forming the silicide layer further comprises forming the silicide layer on the source and drain regions such that the silicide layer extends into the source and drain regions.

3. (Original) The method according to Claim 2, wherein forming the silicide layer further comprises forming a silicide layer that forms a planar junction with the source and drain regions.

4. (Original) The method according to Claim 2, wherein forming the source and drain regions comprises:

forming a lightly doped conductivity type region on both sides of the gate that define the source and drain regions; and

implanting highly doped ions into the lightly doped source and drain regions to provide highly doped portions of the source and drain regions.

5. (Original) The method according to Claim 2:

wherein forming the barrier layer spacer is preceded by forming an insulating layer on the source and drain regions of the integrated circuit substrate; and

wherein forming the barrier layer spacer is followed by removing a portion of the insulating layer from beneath the barrier layer spacer, such that the portion of the barrier layer spacer that protrudes from the sidewalls of the gate extends beyond an end of the insulating layer and a portion of the source and drain regions are exposed, wherein forming the silicide layer further comprises forming the silicide layer on the exposed portion of the source and drain regions.

6. (Original) The method according to Claim 5, wherein forming the barrier layer spacer comprises:

forming spacers on the sidewalls of the gate;

forming a barrier layer on the spacers, the gate and the insulating layer;

forming a sacrificial layer on the barrier layer;

removing a portion of the sacrificial layer exposing a portion of the barrier layer to provide a gate sacrificial spacer; and

removing the exposed portion of the barrier layer to provide a barrier layer spacer and expose a portion of the source and drain regions.

7. (Original) The method according to Claim 6, wherein forming the silicide layer comprises:

forming a silicon epitaxial layer on the exposed portion of the source and drain regions and the barrier layer spacer;

forming a metal layer on the silicon epitaxial layer and the barrier layer spacer; and

thermally treating the metal layer to provide the silicide layer.

8. (Original) The method according to Claim 1, wherein forming a gate comprises:

forming a gate stack pattern including a gate insulating layer on the integrated circuit substrate, a first gate electrode on the insulating layer, a second gate electrode on the first gate electrode, and a capping layer on the second gate electrode.

9. (Original) The method according to Claim 1, wherein the integrated circuit device comprises a dynamic random access memory (DRAM) device.

Claims 10-16 (Canceled).

17. (Original) A method of fabricating an integrated circuit device, comprising:

forming a gate on an integrated circuit substrate, the gate having sidewalls;

forming source and drain regions on the integrated circuit substrate;

forming an insulating layer on a portion of the integrated circuit substrate;

forming a barrier layer spacer on the sidewalls of the gate and the insulating layer;

removing a portion of the insulating layer from beneath the barrier layer spacer, such that the barrier layer spacer extends beyond an end of the insulating layer exposing a lower surface of the barrier layer spacer and a portion of the source and drain regions;

forming a silicide layer on the exposed portions of the source and drain regions.

18. (Original) The method according to Claim 17, wherein forming the silicide layer further comprises forming a silicide layer that extends into the source and drain regions and forms a planar junction with the source and drain regions.

19. (Original) The method according to Claim 17, wherein forming the source and drain regions comprises:

forming a lightly doped conductivity type region on both sides of the gate that define the source and drain regions; and

implanting highly doped ions into the lightly doped source and drain regions to provide highly doped portions of the source and drain regions.

20. (Original) The method according to Claim 19, wherein forming a silicide layer further comprises forming a silicide layer that extends into the highly doped portion of the source and drain regions without extending into the lightly doped portion of the source and drain regions.

21. (Original) The method according to Claim 17, wherein forming a gate comprises:

forming a gate stack pattern including a gate insulating layer on the integrated circuit substrate, a first gate electrode on the insulating layer, a second gate electrode on the first gate electrode, and a capping layer on the second gate electrode.

22. (Original) The method according to Claim 17, wherein forming the barrier layer spacer further comprises:

forming spacers on the sidewalls of the gate;

forming a barrier layer on the spacers, the gate and the insulating layer;

forming a sacrificial layer on the barrier layer;

removing a portion of the sacrificial layer exposing a portion of the barrier layer to provide a gate sacrificial spacer; and

removing the exposed portion of the barrier layer to provide a barrier layer spacer and expose a portion of the source and drain regions.

23. (Original) The method according to Claim 22, wherein forming the silicide layer comprises:

forming a silicon epitaxial layer on the exposed portion of the source and drain regions and the barrier layer spacer;

forming a metal layer on the silicon epitaxial layer and the barrier layer spacer; and

thermally treating the metal layer to provide the silicide layer.

24. (Original) The method according to Claim 17, wherein the integrated circuit device comprises a dynamic random access memory (DRAM) device.

Claims 25-30 (Canceled).

31. (Original) A method of fabricating an integrated circuit device, comprising:

forming a gate on an integrated circuit substrate, the gate having sidewalls; and

forming a barrier layer spacer on the sidewalls of the gate, the barrier layer spacer having a cantilevered portion that extends away from the sidewalls of the gate and exposes a lower surface of the barrier layer spacer that faces the integrated circuit substrate.

32. (Original) The method according to Claim 31 further comprising forming a silicide layer beneath the cantilevered portion of the barrier layer spacer that contacts the exposed lower surface of the barrier layer.

33. (Original) The method according to Claim 32 wherein forming the silicide layer further comprises forming the silicide layer on an upper surface of the cantilevered portion of the barrier layer spacer opposite the lower surface.

34. (Original) The method according to Claim 33 further comprising:

forming a spacer on the sidewalls of the gate, wherein the barrier layer spacer is formed on an outer surface of the spacer; and

forming source and drain regions on the integrated circuit substrate, the source and drain regions having a lightly doped portion and a highly doped portion;

wherein the lightly doped portion extends from outside the gate to beneath the gate, the highly doped portion extends deeper into the substrate than the lightly doped portion, the highly doped portion extends form outside the gate to a boundary of the lightly doped and highly doped portions and the boundary of the lightly doped and highly doped portions extends to between the upper surface of the spacer and a sidewall of the gate contacting an

inner surface of the spacer.

35. (Original) The method according to Claim 34 wherein forming the silicide layer further comprises forming the silicide layer extending into the source and drain region without extending beyond the boundary between the highly doped portion and the lightly doped portion of the source and drain regions.

36. (Original) The method according to Claim 35 wherein forming the silicide layer further comprises forming the silicide layer such that the silicide layer does not extend deeper into the substrate than the lightly doped portion of the source and drain regions and forms a uniform junction with the source and drain regions.

37. (Original) The method according to Claim 36:

wherein forming the barrier layer spacer is preceded by forming an insulating layer on the source and drain regions of the integrated circuit substrate; and

wherein forming the barrier layer spacer is followed by removing a portion of the insulating layer such that the cantilevered portion of the barrier layer spacer extends beyond an end of the insulating layer.

38. (Original) The method according to Claim 37 wherein the end of the insulating layer extends away from the gate beyond the boundary between the lightly doped and highly doped portions of the source and drain regions.

39. (Original) The method according to Claim 38 wherein forming the silicide layer further comprises forming the silicide layer such that the silicide layer does not extend towards the gate beyond the end of the insulating layer.

40. (Original) The method according to Claim 31, wherein the integrated circuit device comprises a dynamic random access memory (DRAM) device.

Claims 41-49 (Canceled).

50. (Original) A method of fabricating an integrated circuit device comprising forming a silicide barrier layer having an end that extends away from a gate beyond a boundary between a lightly doped portion and a highly doped portion of a source and/or drain region that inhibits silicidation thereunder.

51. (Original) The method according to Claim 50, further comprising:

forming a gate on an integrated circuit substrate, the gate having sidewalls; and

forming a barrier layer spacer on the sidewalls of the gate, the barrier layer spacer having a cantilevered portion that extends on the silicide barrier layer away from the sidewalls of the gate.

52. (Original) The method according to Claim 51, wherein forming the barrier layer spacer further comprises forming the barrier layer spacer on the silicide barrier layer such that the cantilevered portion extends beyond an end of the silicide barrier layer exposing a lower surface of the cantilevered portion of the barrier layer spacer facing the substrate.

53. (Original) The method according to Claim 52, further comprising forming a silicide layer on the integrated circuit substrate under the cantilevered portion of the barrier layer spacer such that the silicide layer contacts the lower surface of the cantilevered portion of the barrier layer spacer.

54. (Original) The method according to Claim 53, wherein forming the silicide layer further comprises forming the silicide layer on an upper surface of the cantilevered portion of the barrier layer spacer.

55. (Original) The method according to Claim 54, wherein forming the silicide layer further comprises forming the silicide layer extending into the source and/or drain

region and having an end extending towards the gate without extending past the boundary between the lightly doped portion and the highly doped portion of the source and/or drain region.

Claims 56-61 (Canceled).